IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Currently Amended) A wireless transceiver device, comprising:

modulation circuitry for modulating and demodulating signals that are transmitted over ~~the airwaves~~ airwaves;

frequency conversion circuitry for up converting and down converting between radio frequency signals and baseband frequency signals;

digital-to-analog conversion circuitry for converting from analog to digital and from digital to analog;

a radio controller; ~~and~~

baseband processing circuitry including a first in, first out (FIFO) memory structure for storing addresses for accessing data blocks; and

a plurality of command blocks formed within a memory structure, the command blocks include addresses of data blocks stored within random access memory and a memory portion for storing an indicator for indicating whether a command block of the plurality of command blocks is in use.

Claim 2. (Cancelled)

3. (Currently Amended) The ~~wireless transceiver~~ wireless transceiver device of ~~claim 2~~ claim 1 wherein the ~~first-in, first-out~~ FIFO memory structure includes pointers that define addresses of the command blocks.

Claim 4. (Cancelled)

5. (Currently Amended) The ~~wireless transceiver~~ wireless transceiver device of claim 1 wherein the modulation circuitry includes Gaussian Phase Shift Keying modulation and demodulation circuitry.

6. (Currently Amended) The ~~wireless transceiver~~ wireless transceiver device of claim 1 wherein the frequency conversion circuitry converts directly between radio frequency and baseband.

7. (Currently Amended) A method for storing and transmitting data, comprising:

storing a data block in random access memory; and

storing a pointer that corresponds to the data block in a first in, first out (FIFO) memory structure, the pointer includes an address of a command block;

storing an address of the data block in the command block; and

setting an indicator signal in a defined memory location, wherein the indicator signal indicates that the data block address stored in the command block is for data that has yet to be successfully transmitted and that the command block is busy.

Claims 8-10. (Cancelled)

11. (Currently Amended) The method of ~~claim 10~~ claim 7 wherein an address for a data block is only stored in a command block if ~~an indicator~~ the indicator signal reflects that the command block does not contain the address of a data block that has yet to be successfully transmitted.

12. (Currently Amended) The method of claim 7 further ~~including the step of~~ comprises:

evaluating ~~a command block address stored within a~~ the command block address included within the FIFO pointer.

13. (Currently Amended) The method of claim 12 further ~~including~~ comprises:

examining the contents of the command block specified by the pointer to determine a data block address.

14. (Currently Amended) The method of claim 13 further ~~including the step of~~ comprises:

evaluating at least ~~the first memory location~~ a first memory location of the data block whose address ~~is specified in~~ is stored in the command block to determine ~~the size of the data block~~ a data block size.

15. (Currently Amended) The method of claim 14 further ~~including the step of~~ comprises:

retrieving an amount of data corresponding to the ~~size data block specified in claim 14~~ data block size and transmitting that data to a radio modem for transmission over ~~a wireless airwaves~~ wireless airwaves.

16. (Currently Amended) The method of claim 15 further ~~including the step of~~ comprises:

resetting the indicator signal if the transmission was successful.

17. (Currently Amended) A memory structure formed within a baseband processing system, comprising:

a random access memory portion for storing data blocks that are to be transmitted in a first in, first out (FIFO) order; and a ~~first in, first out~~ FIFO memory structure for storing pointers that correspond to the data blocks stored in the random access memory portion;

a plurality of command blocks defined within the random access memory portion wherein each command block is for specifying an address of a data block that is to be transmitted; and

a defined memory portion for storing command block indicators for each command block, wherein the command block indicators specify whether its corresponding command block includes the address of a data block that has yet to be transmitted successfully.

Claims 18-19. (Cancelled)

20. (Currently Amended) The memory structure of ~~claim 19~~ claim 17 wherein the ~~memory portions~~ defined memory portions for storing the ~~indicators~~ command block indicators are each one bit in length.

21. (Currently Amended) The memory structure of ~~claim 18~~ claim 17 wherein the command blocks defined within the random access memory portions ~~for storing the command blocks~~ are each four bytes in length.

22. (Currently Amended) The memory structure of claim 17 wherein the ~~first in, first out~~ FIFO memory structure defines a plurality of ~~first in, first out~~ FIFO memory blocks wherein each ~~first in, first out memory~~ FIFO memory block relates to data blocks that are to be transmitted to a particular device.